MIL-M-38510/508 15 NOVEMBER 1990

## MILITARY SPECIFICATION

## MICROCIRCUITS, MEMORY, DIGITAL, CMOS ONE-TIME PROGRAMMABLE ARRAY LÓGIC, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

## 1. SCOPE

- $1.1~\underline{Scope}$  . This specification covers the detail requirements for monolithic silicon, CMOS, programmable array logic microcircuits which employ a one-time programmable EPROM cell as the programming element. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN).
  - 1.2 PIN. The PIN shall be in accordance with MIL-M-38510 (see 3.6 herein).
  - 1.2.1 Device types. The device types shall be as follows:

Device type	<u>Circuit</u>	t <sub>PD</sub>
01	22-input, 10-output, AND-OR logic array	30 ns
02	22-input, 10-output, AND-OR logic array	25 ns
03	22-input, 10-output, AND-OR logic array	20 ns
04	22-input, 10-output, AND-OR logic array	15 ns

- 1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.
  - 1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x.100"), square chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to:
Rome Air Development Center, (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

# 1.3 Absolute maximum ratings.

# 1.4 Recommended operating conditions.

Supply voltage range - - - - - - - - - - 4.5 V dc minimum to 5.5 V dc maximum dc maximum low level input voltage (V  $_{\rm IL}$ ) - - - - - 2.0 V dc Maximum low level input voltage (V  $_{\rm IL}$ ) - - - - - 0.8 V dc Case operating temperature range ( $^{\rm T}_{\rm C}$ ) - - - - - - - - - - - - - - - - 55 °C to +125 °C

#### 2. APPLICABLE DOCUMENTS

# 2.1 Government documents.

2.1.1 Specification, standards, and handbooks. The following specifications standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation (see 6.2).

### **SPECIFICATION**

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses less than 20 ns. Maximum output voltage is  $V_{CC}$  + 0.75 V dc which may overshoot

to + 7.0 V dc for pulses less than 20 ns. 2/ Must withstand the added  $P_D$  due to short circuit test; e.g.,  $I_{OS}$ .

## 3. REQUIREMENTS

- 3.1 <u>Detail specifications</u>. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.
- 3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.
- 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

# 3.2.2 Truth table.

- 3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in group A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.
- 3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.
- 3.2.3 <u>Logic diagram</u>. The logic diagram for unprogrammed devices shall be as specified on figure  $\overline{\bf 3}$ .
- 3.2.4 <u>Case outlines</u>. Case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.
- 3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.
- 3.4 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I. The electrical tests for each subgroup are described in table I. Any additional detailed information or electrical test requirements not covered in table I (i.e., pin for pin conditions and testing sequence) shall be maintained and available upon request from the qualifying activity.
- 3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.
- 3.7 <u>Processing options</u>. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.
- 3.7.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 1, 2, and 3 along with 7 and 8 at required access speeds after programming to verify the specific program configuration.

- 3.7.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.
- 3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).
  - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.
- 4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
  - a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.
  - b. Burn-in test, method 1015 of MIL-STD-883.
    - (1) Static test using the circuit shown on figure 5 or equivalent.
      Ambient temperature (TA) shall be +125°C minimum. Test duration
      for the static test shall be 48 hours minimum for class S. The
      48-hour burn-in may, at the manufacturer's option, be broken into two
      sequences of 24 hours each (static I and static II) followed by
      interim electrical measurements.
    - (2) Dynamic test (test condition D or E) using the circuit shown on figure 4 or equivalent. Test duration and temperature shall be in accordance with method 5004 of MIL-STD-883.
  - c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
  - d. Post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.
  - e. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
  - f. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 are performed at the wafer level.)
    - (1) Program 100 percent of the total number of cells, excluding the security bit.
    - (2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.
    - (3) Perform margin test using  $V_m = +5.7 \ V$  at  $+25 \ C$  using loose timing (i.e.,  $t_{ACC} = 1 \ \mu s$ ).
    - (4) Erase.

- 4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 and 8 shall be by attributes only.
- 4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies a device type, then the slower device types of the same die type (see MIL-M-38510) may be part I qualified upon the request of the manufacturer, without any further testing.
- 4.3.2 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.
- 4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).
- 4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:
  - a. Tests shall be as specified in table II herein.
  - b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
  - c. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.
  - d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11.
    - (1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than four total device failures allowable.
    - (2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

- 4.4.2 Group B inspection. Group B inspection shall be in accordance with table II  $\overline{\text{of method 5005 of MIL-STD-883}}$  .
  - a. Class S devices selected for testing in subgroup 5 (table IIa of method 5005 of MIL-STD-883) shall be programmed in accordance with 3.2.2 herein.
  - b. Electrical parameters shall be as specified in table II herein.
  - c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4 or equivalent shall be used.
- 4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:
  - a. End-point electrical tests shall be as specified in table II herein.
  - b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
    - (1) Test condition D or E, using the circuit shown on figure 4 or equivalent.
    - (2)  $T_A = +125$ °C, minimum.
    - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
    - (4) The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of cells programmed.
- 4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:
  - a. End-point electrical tests shall be as specified in table II herein.
  - b. The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of cells programmed.
- 4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.
- 4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.
- 4.6 <u>Inspection of packaging</u>. The sampling and inspection of the preservation, packing and container marking shall be in accordance with the requirements of MIL-M-38510.
- 4.7 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test conditions	   Group A	Device	Limi	ts	Unit
r ar ame ter		$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	subgroups   (test   method)	types	Min	Max	
High level output voltage	v <sub>oH</sub>	$ V_{CC}  = 4.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $ V_{IH}  = 5.0 \text{ V}, I_{OH}  = -2.0 \text{ mA}$	1, 2, 3	   A11 	2.4		٧
Low level output voltage	v <sub>OL</sub>		   1, 2, 3   (3007)	   A11 		0.5	٧
Input high level <u>1</u> /   voltage	V <sub>IH</sub>		1, 2, 3	All	2.0		٧
Input low level <u>1</u> / voltage	V <sub>IL</sub>	V <sub>CC</sub> = 4.5 V	1, 2, 3	   A]] 	 	0.8	V
High impedance output leakage current <u>2</u> /	I I <sub>OZL</sub>	$ V_{CC}  = 5.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $ V_{IH}  = 5.0 \text{ V}, V_{0} = 0.0 \text{ V}$	1, 2, 3	A11   	  -40     	 	   μ <b>A</b>   
High impedance output leakage current <u>2</u> /	l I OZH	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.0 V   V <sub>IH</sub> = 5.0 V, V <sub>O</sub> = 5.5 V	1, 2, 3	   A11     	       	   40   	   μΑ   
High level input	l I IH		1, 2, 3	   All 	   	10	Ι   μΑ 
Low level input	III	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.0 V	1, 2, 3	A11	-10	1   	μA
Supply current	I I CC	V <sub>CC</sub> = 5.5 V   I/O = open   Pins (I <sub>O</sub> -I <sub>11</sub> ) = 0.0 V	1, 2, 3	1   All     	 	  120     	   mA     
Output short circuit current 3/4/	I I <sub>OS</sub>	$V_{CC} = 5.5 \text{ V}, V_0 = 0.5 \text{ V}$	1, 2, 3	   All 	  -30 	  -90   	   mA 
Input capacitance	  C <sub>I</sub> 		   4   (3012)	   A11 	     	   8   	   pF 
Output capacitance	  c <sub>0</sub> 	V <sub>CC</sub> = 5.0 V, V <sub>0</sub> = 0.0 V   T <sub>C</sub> = +25 C, f = 1 MHz   (see 4.4.1c)	(3012)	   A11 	 	   8   	   pF   

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	   Test conditions	Group A		Limi	ts	  Unit
		-55°C < T <sub>C</sub> < +125°C   GND = U V   4.5 V < V <sub>CC</sub> < 5.5 V   unless otherwise specified	subgroups    (test     method)   	types       	Min	Max	     
Input or feedback	t <sub>PD</sub>	  V <sub>CC</sub> = 4.5 V	19, 10, 11	01		30	ns
to nonregistered output		See figure 6 	(3003)   	02		25	
	<b>!</b> <b>!</b>	<u> </u>		03		20	   
	l I	 		04		15	
Clock to output 5/	l t <sub>CO</sub>		9, 10, 11	01		20	ns
	 		(3003) 	02,03		15	   
	 	 		04		1 10	<u> </u>
Input to output enable	l It <sub>PZH</sub>		9, 10, 11	01,02		25	ns
	<del>!</del> !	<u> </u>	(3003)	03		20	-
	i i	<u> </u>		04		1 15	<u> </u>
Input to output enable	  tp <u>ZL</u>		9, 10, 11 (3003)	01,02		25	ns   ns 
 	! !	! !		03	! 	20	
	 	<u>}</u>		04		15	<u> </u>
Input to output	l t <sub>PHZ</sub>		9, 10, 11	01,02	! 	25	ns
disable	1	ļ	(3003)	03	! 	20	<u>.</u>
	<u> </u>	 	 	04	 	15	<u> </u>
Input to output	l  tpLZ		9, 10, 11	01,02	<u> </u> 	25	ns
disable	] [			03	<u> </u>	20	<u>-</u> į
		    -	<u> </u>	04	! 	15	<u> </u>
   Clock pulse width	  t <sub>WH</sub>		9, 10, 11	01	20	<u> </u>	ns
			(3003)	02,03	15	<u> </u>	<u> </u> -
	 	 		04	6	<u>i</u> T	i T
l   Clock pulse width	t <sub>WL</sub>	i 	9, 10, 11 (3003)	01	20	<u>i</u>	ins I
				02,03	15	<u>i</u>	- <u>İ</u> -
<u> </u>	!		<u>i</u>	04	6	<u>i</u>	<u> </u>

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	  Symbol	   Test conditions	Group A	Device	Limi	ts	  Unit
Tul une cer		-55°C < T <sub>C</sub> < +125°C   GND = T V	subgroups   (test	types	Min	Max	   
	l 	4.5 V < VCC < 5.5 V   unless otherwise specified	method) 				<u> </u>
Setup time	l It <sub>S</sub>	  V <sub>CC = 4.5 V                                  </sub>	  9, 10, 11	01	20		ns
	1	lsee figure 6 l	(3003) !	02	18		
	<u> </u> 	 	!	03	17		
	! !	! !		04	10		<u> </u>
Hold time	  t <sub>H</sub> 	  -  -	9, 10, 11	All	0		ns
Maximum clock	l If <sub>MAX</sub>		19, 10, 11	01	25		l   MHz
frequency <u>6</u> /	1	1	(3003) 	l 02	30		
	 	 	 	03	31.2		! !
	 			l l 04	50		 
Asynchronous reset	  t <sub>AW</sub>	1	9, 10, 11 (3003)	01	30	 	ns
pulse width	 	<u> </u>	[ (3003)	02	25	 	
			!	03	20	 	  -
	 	1		04	15	! 	<u> </u>
Asynchronous reset	l It <sub>AR</sub>		9, 10, 11	01	30		ns
recovery time	'	 	(3003) !	02	25		
	 		ļ	03	20		
	<u> </u>	 	 	1   04	15	<u> </u>	<u> </u>
Asynchronous reset to	t <sub>AP</sub>	1	9, 10, 11	01	<u> </u>	30	ns
registered output reset	1	! !	(3003) 	02,03	! 	25	-
	 		<u> </u>	04	<u> </u>	20	<u> </u>

 $<sup>\</sup>underline{1}/$  These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

I/O terminal leakage is the worst case of  $I_{IX}$  or  $I_{O7}$ . For test purposes, not more than one output should be shorted at a time. Short circuit test duration should not exceed one second.

Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

 $<sup>\</sup>frac{5}{6}$ / Test applies only to registered outputs.  $\frac{5}{6}$ /  $f_{MAX}$  is derived by testing  $t_S$  and  $t_{CO}$  and is not tested directly.  $f_{MAX} = 1/(t_S + t_{CO})$ .

TABLE II. Burn-in and electrical test requirements.

Line						Class B devices		
	test method     	Reference paragraph	Table I <u>3/</u> subgroups		    Reference  paragraph	   Table I <u>3</u> /    subgroups	Table III delta 4/l limits	
1	Interim electrical     parameters   (method 5004)		1		 			
2		4.2b	Required		   			
l I 3	  Same as line 1		1*	Δ	 			
4 	  Static burn-in II   (method 1015)	4.2b	   Required 			 		
l I 5	  Same as line 1		1*	Δ		 		
   6 	  Dynamic burn-in   (method 1015)	4.2b	   Required 		4.2b	Required		
l 7	  Same as line 1	4.2d	1*					
8   	  Final electrical   parameters   (method 5004)		  1*,2,3,7,8   <u>5</u> /	Δ	     	1*,2,3,7,8		
   9 	  Group A test   requirements   (method 5005)	4.4.1 	   1,2,3,7,8,   9,10,11	 	4.4.1	1,2,3,7,8, 9,10,11		
10   	  Group B end-point   electrical parameters   (method 5005)	   4.4.2   	1,2,3,7,8, 9,10,11	Ι   Δ 	     	 		
   11 	  Group C end-point   electrical parameters   (method 5005)		     		4.4.3	1,2,3,7,8 5/6/	Δ	
   12 	  Group D end-point   electrical parameters   (method 5005)	   4.4.4   	1,2,3,7,8	     	4.4.4	1,2,3,7,8		

Blank spaces indicate tests are not applicable.

\* indicates PDA applies to subgroup 1 (see 4.2e).

changes which may affect the parameters listed in table III. Delta values shall be computed

with reference to the previous interim electrical parameters.

For subgroups 9, 10, and 11 only, the worst value measured per device need be recorded when variables data is required (e.g., during qualification).

 $<sup>\</sup>Delta$  indicates delta limit shall be required only in table III, subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1). Refer to table III for required parameters and limits to be tested.

The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

For class B, delta limits shall be required on initial qualification or after any design

Device types	01, 02, 03	3, and 04
		3
Case outlines	K, L	
Terminal number	Termina	symbol
1	CP/I <sub>O</sub>	NC
2	11	CP/I <sub>O</sub>
3	I <sub>2</sub>	<sup>I</sup> 1
4	13	12
5	14	I3 !
6	I <sub>5</sub>	14
7	1 <sub>6</sub>	I <sub>5</sub>
8	17	NC
9	I <sub>8</sub>	<sup>1</sup> 6
10	l Ig	17
11	I <sub>10</sub>	18
12	GND	19
13	I I11	1 <sub>10</sub>
14	1/00	GND
15	1/01	į nc į
16	1/02	I <sub>11</sub>
17	1/03	1/00
18	1/04	1/01
19	1/05	1/02
20	1/06	1/03
21	1/07	1/04
22	1/08	NC
23	1/09	1/05
24	V <sub>CC</sub>	1/06
25	i	1/07
26	1	1/08
27	İ	1/09
28		VCC

FIGURE 1. Terminal connections.

	Truth table																				
				Inpu												Output					
CP/IO	11	12	13	14	15	16	17	18	19	I <sub>10</sub>	I <sub>11</sub>	1/00	1/01	1/02	1/03	1/04	I/05	1/06	1/07	1/08	1/09
i	x					_				χ			Z	Z		Z	Z	Z	Z	Z	Z

NOTES:
1. Z = High impedance
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).

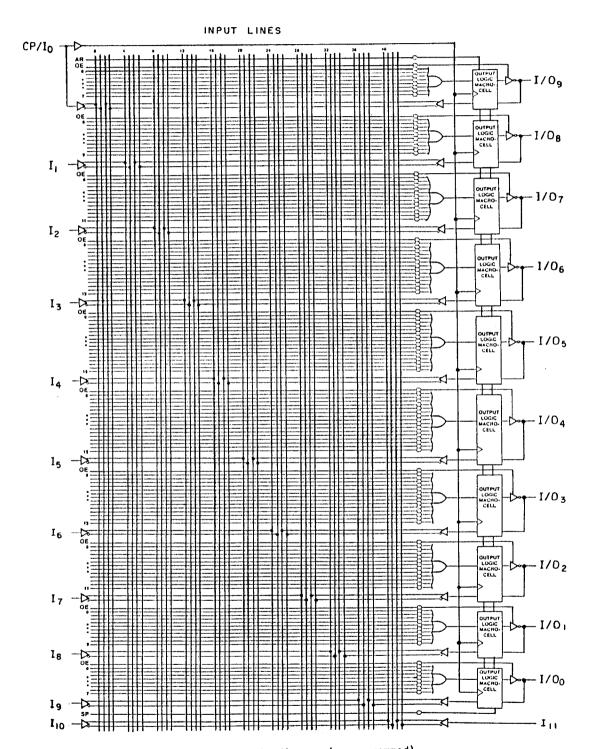


FIGURE 3. Logic diagram (unprogrammed).

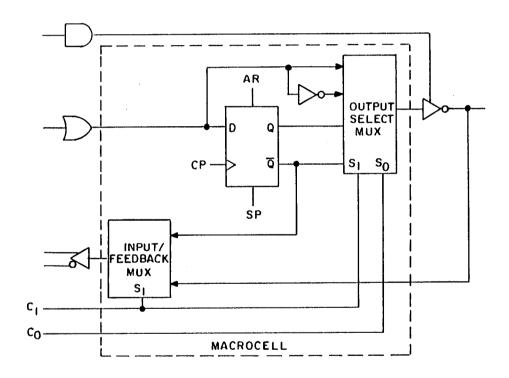
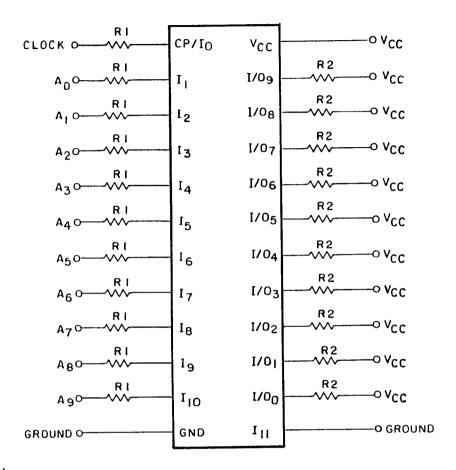


FIGURE 3. Logic diagram (unprogrammed) - Continued.



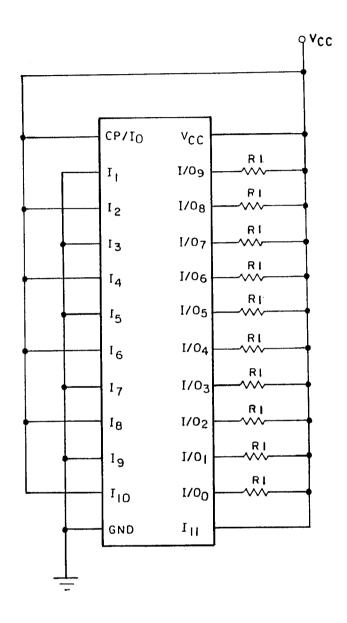
## NOTES:

- R1 = 1 k $\Omega$  ±5% and is located on the program board. Each R1 feeds a maximum of 420 1.

- 2. R2 = 1 k $\Omega$  ±5% and is located at each device pin. 3. There is one 0.1  $\mu F$  decoupling capacitor on every socket between VCC and ground. 4. All pulse generators have the following characteristics: VIL = -0.25 V minimum to 0.25 V maximum; VIH = 2.75 V minimum to 3.25 V maximum; 50% duty cycle and frequencies as specified in note 6. 5. VCC = 5.75 V ±0.25 V.
- 6. Input frequencies are as follows:

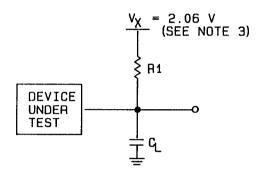
Input	Frequency (±50%)	Input	Frequency (±50%)
CLOCK	$f_0 = 500 \text{ kHz}$	A <sub>5</sub>	$f_6 = 1/64 f_0$
A <sub>O</sub>	$f_1 = 1/2 \ f_0$	A <sub>6</sub>	$f_7 = 1/128 \ f_0$
$A_1$	$f_2 = 1/4  f_0$	A7	$f_8 = 1/256 \ f_0$
A <sub>2</sub>	$f_3 = 1/8 \ f_0$	8A	$f_9 = 1/512 \ f_0$
A <sub>3</sub>	$f_4 = 1/16 \ f_0$	A <sub>9</sub>	$f_{10} = 1/1024 f_0$
Aα	$f_5 = 1/32  f_0$		

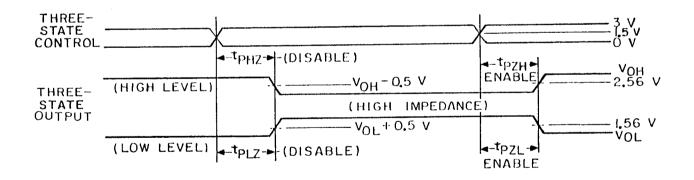
FIGURE 4. Burn-in and life test circuit.



- NOTES: 1. R1 = 1 k $\Omega$  ±5%. 2. V<sub>CC</sub> = 6.50 V ±0.25 V. 3. For static II burn-in, reverse all input connections (i.e., V<sub>SS</sub> to V<sub>CC</sub> and V<sub>CC</sub> to V<sub>SS</sub>).

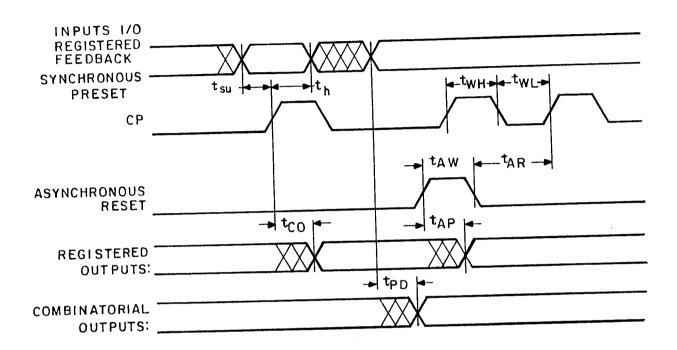
FIGURE 5. Static burn-in circuit.





OUTPUT CONTROL SWITCHING WAVEFORM

FIGURE 6. Switching time test circuit and waveforms.



NOTES: 1.  $C_L$  = 50 pF minimum, including jig and probe capacitance.  $t_{PHZ}$  and  $t_{PLZ}$  are specified with  $C_L$  = 5 pF.

R1 = 105 ohms  $\pm 1$  percent.

2.  $V_{IH}$  = 3.0 V,  $V_{IL}$  = 0.0 V. 3. For tp<sub>ZH</sub>, tp<sub>ZL</sub>, tp<sub>HZ</sub>, and tp<sub>LZ</sub>:

Test	<u>v</u> x	Output measurement level
tpzh	2.06	2.56 V
tpzl	2.06	1.56 V
tphz	1.5	V <sub>OH</sub> -0.5 V
<sup>t</sup> plz	2.60	V <sub>OH</sub> +0.5 V

FIGURE 6. Switching time test circuit and waveforms - Continued.

TABLE III. Delta limits at +25°C.

Parameter <u>1</u> /	Device types
	<u>  All</u>
ICC	   ±2 mA 
I OZH I OZL	t ±10% of specified value
I I I H	±10% of   specified   value

 $\frac{1}{2}$  The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (  $\Delta$  ).

#### 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

- $6.1\ \underline{Intended\ use}$ . Microcircuits conforming to this specification are intended for use for original equipment design application and logistic support of existing equipment.
  - 6.2 Acquisition requirements. Acquisition documents must specify the following:
    - a. Title, number, and date of the specification.
    - Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).
    - c. Complete PIN (see 1.2).
    - d. Requirement for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
    - e. Requirement for certificate of compliance, if applicable.
    - Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
    - g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
    - h. Requirements for product assurance options.

- i. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- j. Requirements for programming the device, including processing option.
- k. Requirements for "JAN" marking.
- 6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - - - - - - Ground zero voltage potential.

 $V_{IN}$  - - - - - - - - - Voltage level at an input terminal.

 $I_{IN}$  - - - - - - - - Current flowing into an input terminal.

- 6.4 Logistic support. Lead material and finish (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the PIN. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.
- 6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military	Vendor similar
device type	PIN
01	C22V10-30
02	C22V10-25
03	C22V10-20
04	C22V10-15

## CONCLUDING MATERIAL

Custodians: Army - ER Navy - EC Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 19, 85, 99
DLA - ES

User activities: Army - SM Navy - AS, CG, MC Preparing activity: Air Force - 17

Agent: DLA - ES

(Project 5962-1208)